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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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BURNS DOANE SWECKER & MATHIS L L P
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404

| EXAMINER | |
|---|---|
| CONNOLLY, MARK A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2115 | |

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/679,398 | PHILLIPS ET AL. | |
| | Examiner | Art Unit | |
| | Mark Connolly | 2115 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 5-7,11-13 and 15-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 5-7, 11-13, 15-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 5-7, 11-13, 15-22 have been presented for examination.

2. Claims 15, 16 and 18 have been amended.

3. Claim 14 has been canceled without prejudice

4. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 5 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Greenbaum et al [Greenbaum] US Pat No 6077315.

7. Referring to claim 5, Greenbaum explicitly teaches an on-chip configuration cache (204) containing a multiplicity of stored configurations (116) [figs. 1 and 2 and col. 5 lines 59-65]. Although Greenbaum is not explicit that each configuration is identified by a unique off-chip address used to fetch that configuration, it is inherent that data stored in a cache is identified by the data's unique address in external memory, which is translated into an address location in the cache. The unique address in external memory is interpreted as a unique off-chip address because the memory is separate from the cache.

8. Referring to claim 20, Greenbaum explicitly teaches an on-chip configuration cache (204) containing a multiplicity of stored configurations (116) [figs. 1 and 2 and col. 5 lines 59-65]. Although Greenbaum is not explicit that each configuration is identified by a unique off-chip address used to fetch that configuration, it is well known that data stored in a cache is identified by the data's unique address in external memory, which is translated into an address location in the cache. The unique address in external memory is interpreted as a unique off-chip address because the memory is separate from the cache. In addition, Greenbaum further teaches that additional configurations (116) are stored in an external memory (104) [col. 5 lines 59-65 and fig. 1].

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 6, 11-13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greenbaum as applied to claims 5 and 20 above, and further in view of Singh et al [Singh] US Pat No 6324621.

11. Referring to claim 6, although Greenbaum teaches that configurations are stored in a cache, it is not explicitly taught that the configurations within the cache are compressed. Singh explicitly teaches a cache which stores compressed data [col. 1 lines 41-43, col. 2 lines 16-19 and figs. 1 and 5B]. It would have been obvious to one of ordinary skill in the art to modify the Greenbaum system to compress the configurations stored within the cache because it would

improve "performance on par with increasing a cache's size without incurring the cost expense of the cache size increase" as is explicitly taught by Singh [col. 2 lines 18-20].

12. Referring to claims 11 and 12, although Greenbaum teaches a configuration cache [204 fig. 2], it is not explicitly taught that the configuration includes a compressed and decompressed cache. Singh explicitly teaches a cache which includes a compressed and decompressed cache [col. 3 lines 4-12 and figs. 1 and 5B]. It would have been obvious to one of ordinary skill in the art to modify the Greenbaum system to include a compressed and decompressed cache because it would improve "performance on par with increasing a cache's size without incurring the cost expense of the cache size increase" as is explicitly taught by Singh [col. 2 lines 18-20].

13. Referring to claim 13, Singh explicitly teaches that data read from the cache is read from the decompressed cache (L3) [col. 4 lines 31-39]. Therefore it is obvious that in the Greenbaum-Singh system, the active configuration plane reads and uses configuration content that is stored in the decompressed cache. The active configuration plane is interpreted as the Reconfigurable Logic Resources 202 that is configured by configuration cache 204 in fig. 2 in Greenbaum.

14. Referring to claim 15, this is rejected on the same basis as set forth hereinabove. It is interpreted that the configuration content is promoted from the decompressed cache when it is used to configure the active configuration plane.

15. Referring to claim 16, Greenbaum explicitly teaches an on-chip configuration cache (204) for configuring an active configuration plane (202) [figs. 1 and 2 and col. 5 lines 59-65]. Although Greenbaum is not explicit that each configuration is identified by a unique off-chip address used to fetch that configuration, it is inherent that data stored in a cache is identified by the data's unique address in external memory, which is translated into an address location in the

cache. The unique address in external memory is interpreted as a unique off-chip address because the memory is separate from the cache. Greenbaum does not explicitly teach that the system includes a compressed and decompressed cache wherein compressed configuration content is decompressed from the compressed cache into the decompressed cache and wherein the decompressed configuration in the decompressed cache is used to configure an active configuration plane. Singh explicitly teaches a compressed and decompressed cache wherein compressed data is decompressed from the compressed cache into the decompressed cache [col. 3 lines 4-12, col. 4 lines 31-39 and figs. 1 and 5B]. It would have been obvious to one of ordinary skill in the art to modify the Greenbaum system to include a compressed and decompressed cache to store the configuration content because it would improve "performance on par with increasing a cache's size without incurring the cost expense of the cache size increase" as is explicitly taught by Singh [col. 2 lines 18-20].

In addition, Singh explicitly teaches that data read from the cache is read from the decompressed cache (L3) [col. 4 lines 31-39]. Therefore it is obvious that in the Greenbaum-Singh system, the active configuration plane reads and uses configuration content that is stored in the decompressed cache.

16. Referring to claims 17, 21 and 22, these are rejected on the same basis as set forth hereinabove.

17. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Greenbaum as applied to claims 5 and 20 above, and further in view of Silberman et al [Silberman] US Pat No 6088763.

18. Referring to claim 7, Greenbaum does not explicitly teach address identification through the use of a content-addressable memory. Silberman teaches that when accessing a cache, an address translation occurs [col. 1 lines 34-37]. Silberman further teaches that this address translation can be improved by employing a content-addressable memory (CAM) [col. 1 lines 42-45]. It would have been obvious to one of ordinary skill in the art to include the address translation means through the use of a CAM as taught by Silberman in the Greenbaum system because it would "improve the translation process" as is explicitly taught by Silberman.

19. Claims 18 and 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Greenbaum and Singh as applied to claims 5-6, 11-17 and 20-22 above, and further in view of Yoshida US Pat No 5951708.

20. Referring to claim 18, although the Greenbaum-Singh system teaches an on chip decompressed cache for storing configuration content, Greenbaum and Singh do not explicitly teach decoding configuration content from the on-chip decompressed cache. In summary, the Greenbaum-Singh system is silent on decoding the compressed data. Yoshida explicitly teaches decoding compressed data [col. 5 lines 32-42]. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the decoding means taught in Yoshida into the Greenbaum-Singh system because it would provide a means to detect any errors in the configuration content.

21. Referring to claim 19, it is obvious that only the portions of the configuration within the reconfigurable chip which need to be reconfigured will be changed because it is well known in the art that overwriting data with identical data is redundant and decreases performance.

***Response to Arguments***

22. Applicant's arguments filed 25 October 2004 have been fully considered but they are not persuasive.

23. In the remarks, applicants argued in substance that Greenbaum US Pat No 6077315 fails to teach the claimed feature wherein "wherein each configuration is identified by a unique off-chip address used to fetch that configuration."

24. Greenbaum explicitly teaches caching configurations within the configuration cache 204 in order to prevent having to reload previous configurations from the configuration portion 116 of the external memory 104. A configuration is loaded through the use of the instruction *gaconf reg* which loads a configuration at a given *address* [see TABLE 1]. The examiner took the position that it was inherent that the configurations stored on the on-chip configuration cache 204 were identified by a unique off-chip address used to fetch that configuration because caching schemes use a unique off-chip address to store and fetch data; or in this case configuration data used to configure the reconfigurable computing chip. In this argument, configuration data and data are interpreted as being the same. When fetching data from a cache, the address of where that data is located in external main memory is used. A predetermined number of least significant bits of the address, commonly referred to as an index, are used in order to reference a particular address within the cache while the rest of the address which comprises the most significant bits of the address, commonly referred to as a tag, are used to compare with a corresponding tag in the cache associated with the cache address referenced by the index. Once the cache address is referenced and it is determined that the tag values are equal, then the data is *identified* as being valid and the data can be loaded. This prevents the system from having to

fetch the data from external memory. The address used to fetch the configuration from memory 104 is interpreted as an *off-chip address* since the address is intended for the configuration portion 116 of memory 104 which is *off-chip*. Furthermore, because the off-chip address is intended to be used to identify the configuration in memory 104 and only the configuration at that address location, the address is interpreted as *unique*. Since the same address is used to identify a cached configuration in configuration cache 204, it is interpreted that those individual cached configurations are also identified by unique off-chip addresses since both the indexes and tags, which make up the unique addresses, are both used to identify the configuration within the cache. Because caches are designed to hold the same amount of data at each cache address as is stored in each address of external memory and because Greenbaum suggests that an entire configuration is stored at a single address in external memory, it is further interpreted that multiple addresses are not required to load a configuration from the configuration cache.

***Conclusion***

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. US Pat No 5696929 to Hasbun et al teaches that the size of each cache lines vary depending on the data being written into them [col. 4 lines 30-33].

b. US Pat No 5835929 to Gaskins et al teaches that the size of a cache line varies from system [col. 3 lines 12-15].

c. US Pat No 5996061 to Lopez-Aguado et al teaches the size of the DATA field in a cache line varies with the line size in external memory [col. 10 lines 5-8].

d. US Pat No 6021466 to Olarig teaches the length of the cache lines vary from cache to cache [col. 1 lines 46-49].

e. US Pat No 6092141 to Lange teaches that a cache line size can be any binary multiple [col. 17 lines 4-6].

f. US Pat No 6122708 to Faraboschi et al teaches that the number of bytes in a cache line can vary [col. 8 lines 42-43].

g. US Pat No 6253299 to Smith et al teaches that the width of cache lines vary to accommodate different data [col. 6 lines 16-20].

h. US Pat No 6556952 to Magro teaches that it is well known that a cache line size is defined by design requirements and can vary greatly in size [col. 9 lines 4-6].

i. US Pat No 6725343 to Barroso et al teaches that the size of a cache line will vary from one implementation to another [col. 8 lines 23-28].

j. US Pat No 6725336 to Cherabuddi teaches that the cache line size can be any suitable length [col. 5 lines 30-31].

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mark Connolly
Examiner
Art Unit 2115

mc
November 8, 2004